Neo-Iso™ TS13101
Galvanic Isolated Latching 60V Solid State Relay

TRIUNE PRODUCTS

Features

- Low Quiescent Operating Currents
  2uA/4uA in OFF/ON state
- Scalable galvanic isolation from primary to secondary sides of the device
- Single control signal for on/off input (CLK)
  Operation from 2.7V to 5.5V
  Compatible with standard microcontrollers
- Switch Characteristics
  High voltage switch with bi-directional blocking in OFF state
  60V switch and 110mΩ $R_{DS(on)}$
  Up to 4A operating current
- Transient protection for SW1 and SW2 to:
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns) level 4
  IEC 61000-4-5 (Surge/Lightning) 160V with 2Ω internal impedance (1.2/50µs)

Specification

- Junction operating temperature -40°C to 125°C
- Packaged in a 20 pin QFN (4x4)
- Product is lead-free, Halogen Free, RoHS / WEEE compliant

Description

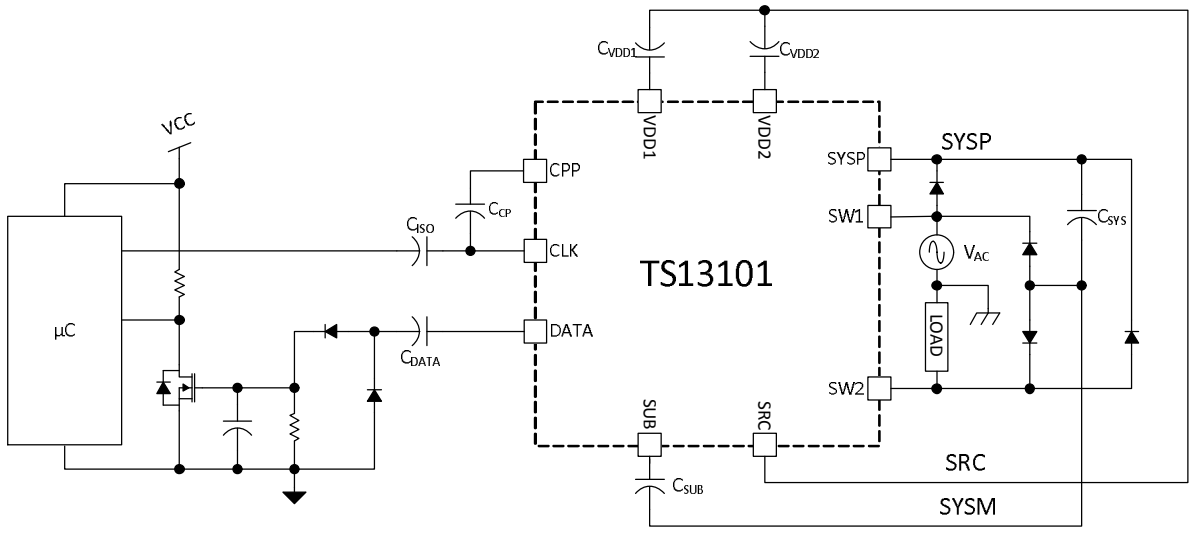
The TS13101 is a galvanically isolated 60V solid state relay with bi-directional blocking. The device includes a single integrated 110mΩ high voltage switch allowing high efficiency switching of power loads or other high current applications. The input pin, CLK, controls the turn on/off of the switch. When the correct CLK sequence is provided the switch will latch on and stay on until the turn off sequence is given or a fault is detected.

The TS13101 includes several protection features. Each switch has an integrated over-current shut-down to prevent device damage during short-circuit or other unusually high load conditions. If an over-current event is detected for a time, the FET is latched off until the CLK turn on sequence is given. While the CLK pin is active after an over-current event or in the event of an incorrect turn-on sequence, the DATA pin is toggled at ¼ the CLK frequency.

Applications

- Power load/rail switching
- Input supply multiplexing
- Isolated power supplies
- Solid state relays
- HVAC control

TYPICAL APPLICATION CIRCUIT



PIN DESCRIPTION

Pin #	Pin Name	Pin Function	Description
1	SRC	Switch Driver Supply Return	Local common supply return
2	SW2	Switch Output Node 2	
3	SW1	Switch Output Node 1	
4	SW1	Switch Output Node 1	
5	SW2	Switch Output Node 2	
6	SW1	Switch Output Node 1	
7	SW2	Switch Output Node 2	
8	SW2	Switch Output Node 2	
9	DATA	Data Output	AC Coupled Data Output
10	CLK	Clock Input	AC Coupled Clock and Power Input
11	SYSP	Positive System Voltage	
12	CPP	Charge Pump Cap	Additional Cap used for lower voltage Clock drive
13	VDD1	Internal Supply 1	Bypass Capacitor for Internal Supply
14	VDD2	Internal Supply 2	Bypass Capacitor for Internal Supply
15	NC	No Connect	
16	SUB	IC Substrate Bias	Connect C_{SUB} Capacitor to SYSM
17	NC	No Connect	
18	SW1	Switch Output Node 1	
19	SW1	Switch Output Node 1	
20	SW2	Switch Output Node 2	
PAD	PAD	Power PAD	Must be floating or connected to SUB

FUNCTIONAL BLOCK DIAGRAM

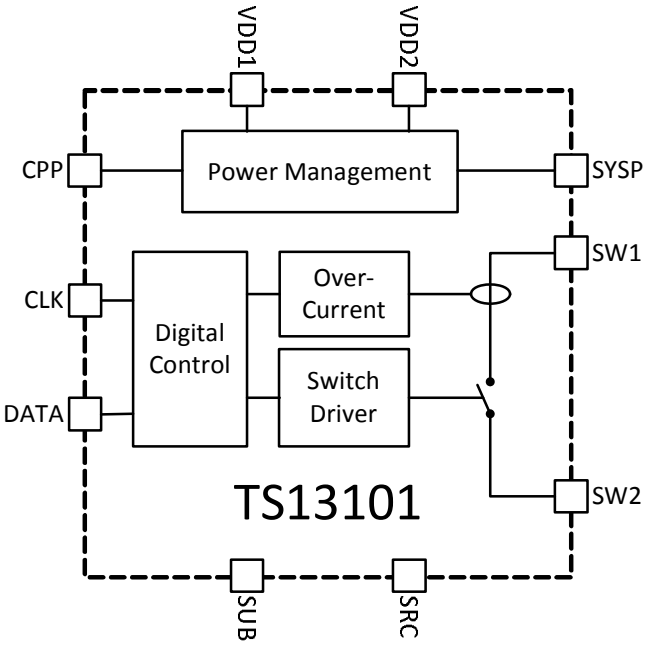


Figure 1: TS13101 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Over operating free–air temperature range unless otherwise noted. (1, 2, 3)

Parameter	Range	Unit
SW1, SW2, SYSP (Peak Voltage, with respect to SUB, SRC)	-0.5 to 60	V
SW1, SW2 (with respect to each other)	-60 to 60	V
CLK, DATA, VDD1, VDD2, CPP (with respect to SUB, SRC)	-0.3 to 5.5	V
SUB	-60 to 0.3	V
Maximum Junction Temperature, $T_{J\,MAX}$	150	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2	kV
Electrostatic Discharge – IEC Contact (SW1 and SW2 Pins)(4)	±30	kV
Electrostatic Discharge – IEC Air Discharge (SW1 and SW2 Pins)(4)	±30	kV
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to SRC terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard

(4) IEC ESD testing is performed on Semtech Product Evaluation Board TS13101-EVMX3.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction to Air (Note 1)	25	°C/W
Θ_{JC}	Thermal Resistance Junction to Case (Note 1)	2.5	°C/W
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 20LD 4x4 QFN with hi-K JEDEC board and 13.5 inch2 of 1 oz. Cu and 4 thermal vias connected to PAD

RECOMMENDED OPERATING CONDITIONS

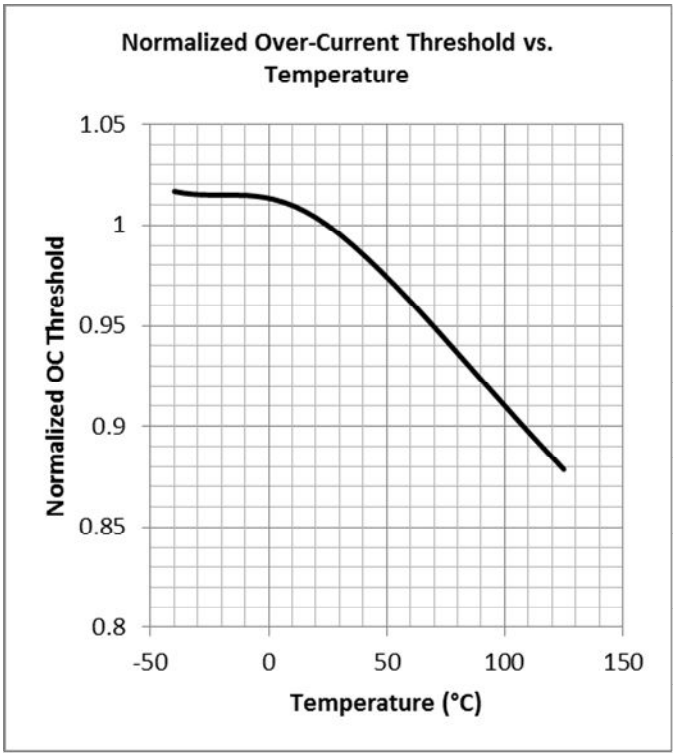
Symbol	Parameter	Min	Typ	Max	Unit
V_{SW}	AC Switch Voltage (RMS Voltage)	-36		36	V
V_{SW}	DC or AC Peak Switch Voltage	-51		51	V
C_{DATA}	Data Isolation Capacitor		100		pF
C_{ISO}	Clock Isolation Capacitor		680		pF
C_{CP}	Charge Pump Capacitor		100		pF
C_{VDD1}	VDD1 Bypass Capacitor		10		nF
C_{VDD2}	VDD2 Bypass Capacitor		1		µF
C_{SUB}	Sub Capacitor		100		nF
C_{SYS}	System Bypass Capacitor		100		nF
CLK Drive					
V_{CLK}	Clock Drive Voltage; Amplitude of driven CLK signal, Drive Impedance < 100Ω	2.7		5.5	V
F_{CLK}	Clock Frequency to Turn on Switch	500		2000	kHz
$N_{CLKON-INIT}$	Number of CLK pulses to initialize Turn On	3		8	pulses
T_{LOW-ON}	CLK Low time during Turn On Sequence	10		20	µs
N_{CLKON}	CLK Pulses to Turn on SW After T_{LOW-ON}	15			pulses
$T_{CLKOFF-INIT}$	CLK Low time to Initialize Turn-Off	10		20	µs
N_{CLKOFF}	CLK Pulses to Enable Turn-Off After $T_{CLKOFF-INIT}$	6		13	pulses
$N_{CLK-OFFDET}$	CLK Pulses to Detect Incorrect Turn-On Sequence	19			pulses
$T_{PRE-CHG}$	Pre-Charge Time for VDD1, VDD2 when $\lvert V_{SW2}-V_{SW1}\rvert<5.0V$ V_{CLK} = 3.0V, F_{CLK} = 1MHz	50			ms

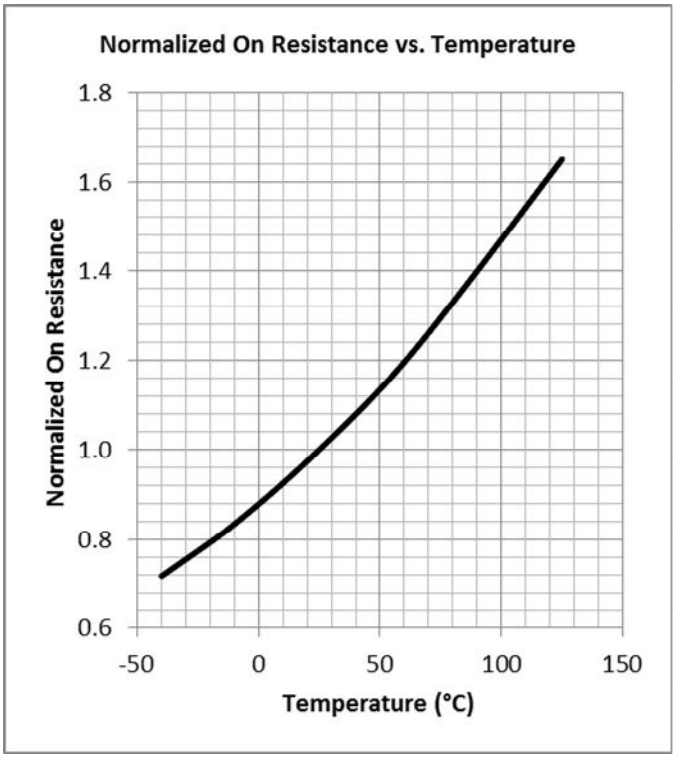
ELECTRICAL CHARACTERISTICS

Electrical Characteristics, T_J = -40°C to 125°C (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage						
$I_{CLK-NORM}$	Normal Mode, CLK running	V_{CLK} = 5.0V, F_{CLK} = 500kHz		15		µA
$I_{CLK-NORM}$	Normal Mode, CLK running	V_{CLK} = 3.0V, F_{CLK} = 1000kHz		50		µA
$I_{CLK-STBY}$	Quiescent current	V_{CLK} = 0V, C_{ISO} = 680pF		3		µA
I_{SYSP}	Quiescent current	T_J < 85°C, Latch Mode		3	20	µA
DATA Output						
F_{DATA}	Data Frequency during Current Shutdown			F_{CLK}/4		kHz
Output Switch						
$R_{DS(on)}$	On Resistance	T_J= 25°C	85	110	135	mΩ
I_{OFF}	Off State Leakage	V_{SYS} = V_{SW}, T_J< 85^{0}C		0.01	3	µA
I_{OUTOC}	Over Current Shutdown	T = 25°C		5.5		A
OC_{FILT}	Output Over Current Deglitch			25		µs
V_{CLAMP}	Differential SW1/2 Clamping Voltage	(SW1-SW2) or (SW2-SW1) I_{SW} = 50mA	58	63	68	V
T_{CLKOFF}	Time for Turn Off		4		10	µs

PRODUCT CHARACTERISTICS





APPLICATION WAVEFORMS

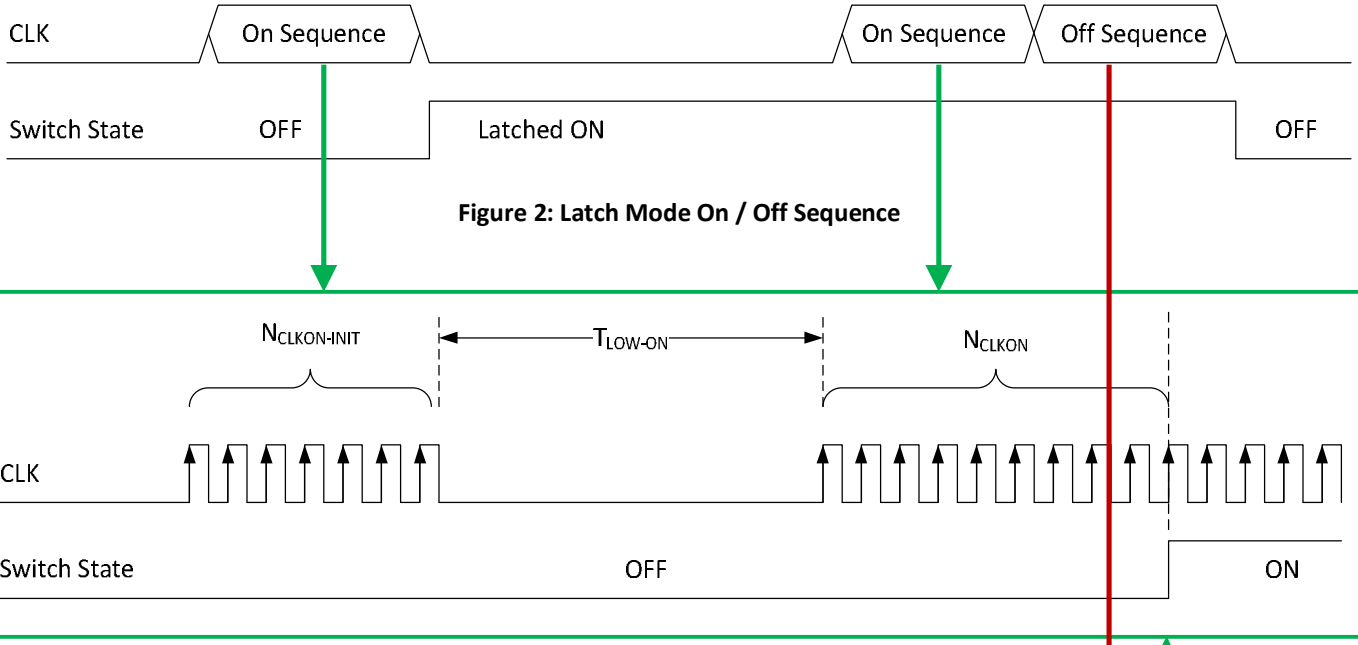


Figure 2: Latch Mode On / Off Sequence

Figure 3: CLK Turn-On Sequence

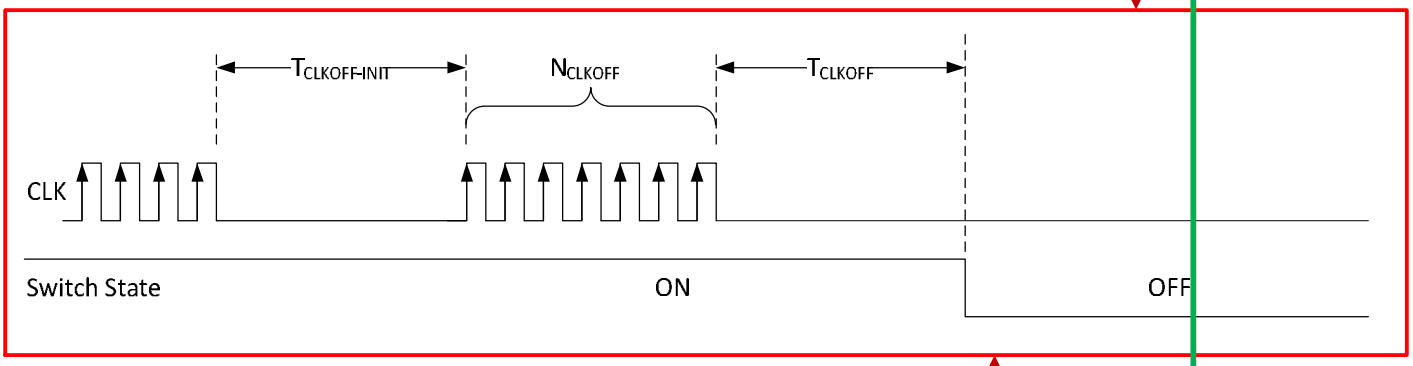


Figure 4: CLK Turn-Off Sequence

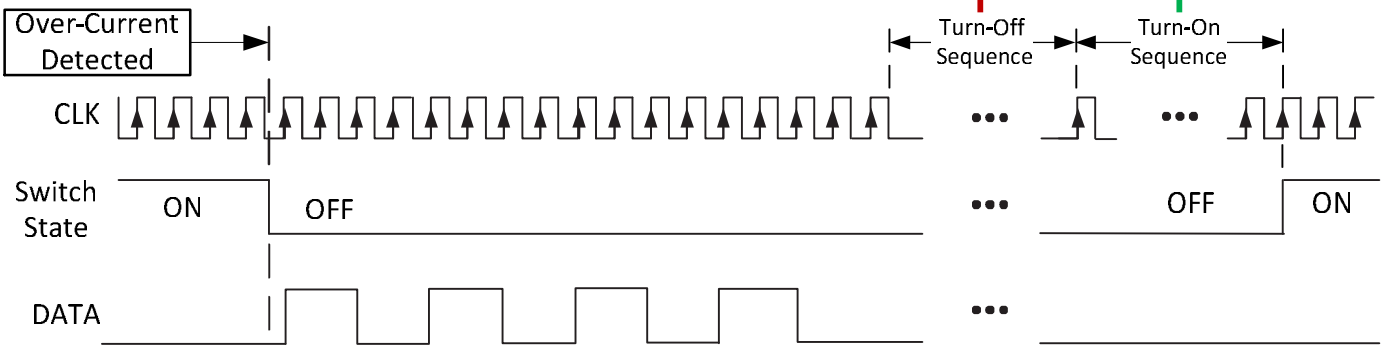


Figure 5:Over-Current Shut-Down and Restart

SWITCH CONTROL

The TS13101 CLK pin performs a dual function:

1. It provides the command sequences in level and timing that determine the state of the switch.
2. It provides a source of power by which the switch can operate.

The microcontroller provides the CLK signal to the switch by a coupling capacitor, C_{ISO}, that provides galvanic isolation between the microcontroller supply domain and that of the switch, the latter of which has a different reference voltage with respect to ground dependent on its state. Because of the requirement to source power, it is required that the microcontroller has a maximum source impedance of 100Ω.

The CLK pin is used as a means to command the state of the switch by the ON and OFF sequences shown in Figure 2 through Figure 5. Figure 2 shows the state of the switch being changed by sending ON and OFF Sequences. On initial power up, the switch state will default to the OFF condition.

It is necessary to send a device ON Sequence to transition the device to the ON state, as shown in Figure 3. First a series of clocks, $N_{CLKON-INIT}$, of frequency F_{CLK} is transmitted, followed by a CLK low time of T_{LOW-ON}. Then another series of clocks of number N_{CLKON} is transmitted. On the final CLK edge the switch will be closed. Note that the CLK continues to cycle and the state of the DATA pin continues to be low. This indicates that the device is ON.

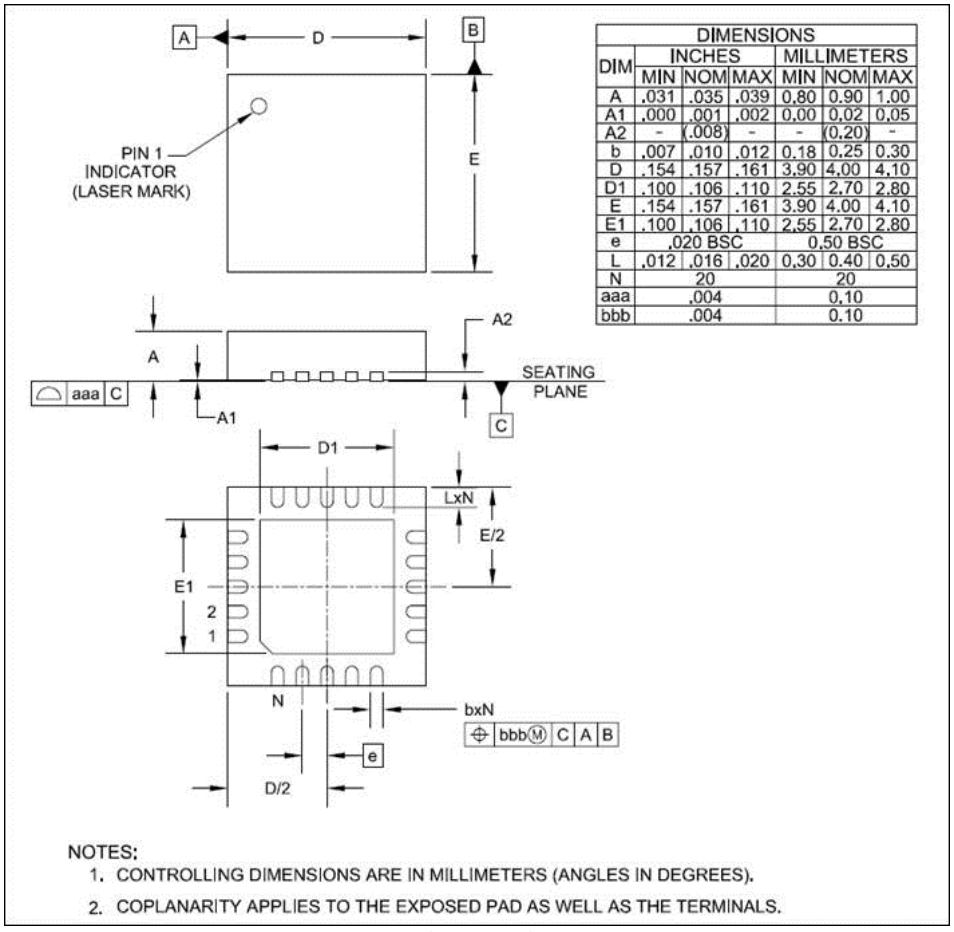
When it is desired to transition the device to the OFF state, the OFF Sequence must be transmitted via the microcontroller. This sequence is shown in Figure 4. Here the CLK is stopped for a period of $T_{CLKOFF-INIT}$, followed by a series of clocks of number N_{CLKOFF}. Then the CLK must be asserted low for a period T_{CLKOFF}, after which the switch will be opened. If the CLK resumes switching, the DATA pin will return a signal F_{CLK} / 4, indicating that the state of the switch is OFF.

Figure 5 shows the operation when an over-current event is detected, and the device autonomously transitions to the OFF state in order to protect itself and the load in the system. During the ON time, the CLK was being switched and the DATA pin was static, being held by the device in the low state. After the over-current event opens the switch, the DATA pin will start switching at F_{CLK} / 4 to signal the microcontroller that the switch is no longer in the ON state. The microcontroller may infer from this that there has been a fault in the system. If diagnostics (performed elsewhere in the system) determine that the fault condition has been removed, the device may be returned to the ON state through the restart sequence shown. After an over-current event opens the switch, an OFF Sequence must be registered in the part before an ON Sequence can successfully transition the device back to the ON state. The DATA pin will assert low and stay low after the ON Sequence as long as load current remains below I_{OUTOC}. If the switch transitions to the closed state and an over-current condition is detected, the process of Figure 5 will repeat.

Failed Communication

In the event of a failed ON command sequence (due to external interference, system transients, etc.) the DATA pin will begin sending a signal at frequency F_{CLK} / 4. Thus the microcontroller is alerted to a communication failure. Similarly, when an OFF command sequence has been sent, resuming CLK pulses after the T_{CLKOFF} time will result in the DATA pin sending a signal of frequency F_{CLK} / 4. If the DATA pulses do not commence after 23 CLK cycles, the microcontroller can discern that the OFF sequence was not received correctly and the switch is still in the closed state. It is up to the microcontroller to do this fault handling and rectify the situation.

PACKAGE INFORMATION



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.154	.157	.161	3.90	4.00	4.10
D1	.100	.106	.110	2.55	2.70	2.80
E	.154	.157	.161	3.90	4.00	4.10
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	20			20		
aaa	.004			0.10		
bbb	.004			0.10		

Figure 6: Package Outline Drawing

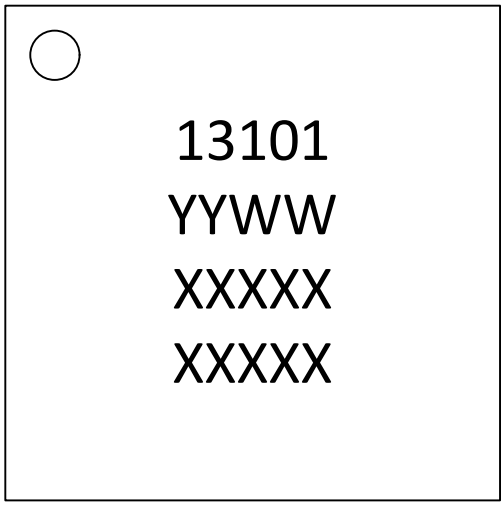
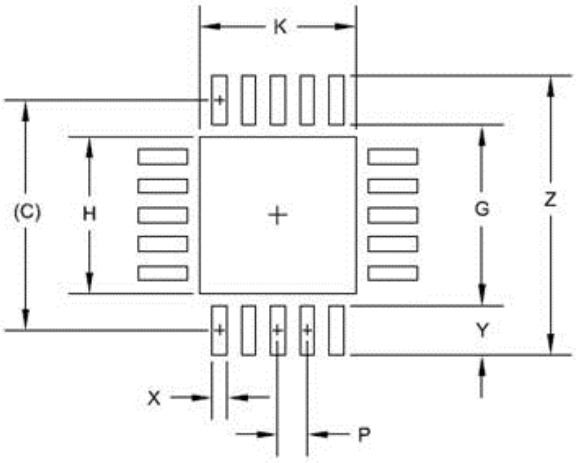


Figure 7: Device Symbolization

Notes:
YYWW = Year Calendar Week
XXXXX = Semtech Lot Number
XXXXX = Lot Number (Continued)



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 8: Recommended Board Layout Land Pattern

ORDERING INFORMATION

Part Number	Description	Package
TS13101-QFNR	Latching Galvanic Isolated Switch	20-pin PQFN Reel (3,300 pcs)

CONTACT INFORMATION

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